

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jun-Fei Zheng et al.

Serial No.: Not yet assigned

Filed: Herewith

For: WORK FUNCTION TUNING FOR
MOSFET GATE ELECTRODESAssistant Commissioner for Patents
and Trademarks
Washington, D.C. 20231

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) Examiner: Not yet assigned

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) Art Unit: Not yet assigned

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(Signature of person mailing paper or fee)February 6, 2002
(Date signed)FORMAL DRAWINGS SUBMISSION

Enclosed herewith for submission in the United States Patent and Trademark
Office are five (5) sheets of formal drawings for the patent application referenced above.

If there are any further charges please charge them to Deposit Account No. 02-
2666. A duplicate of this sheet is enclosed for that purpose.

Respectfully submitted,

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Fig. 1

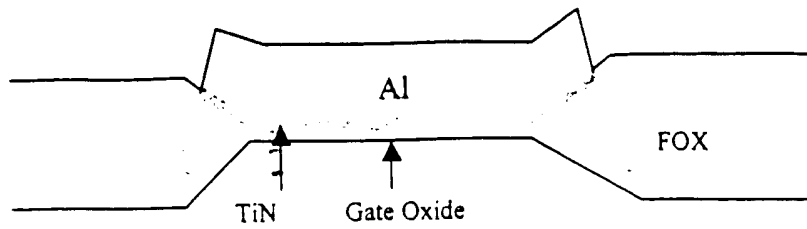


Fig. 2

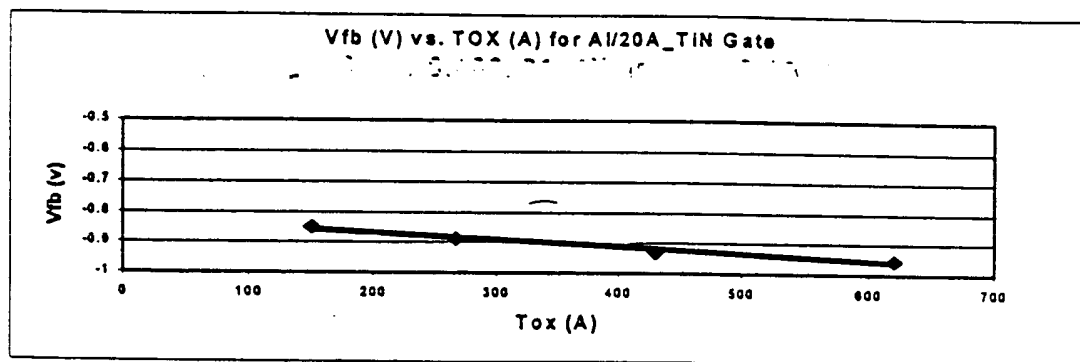


Fig. 3

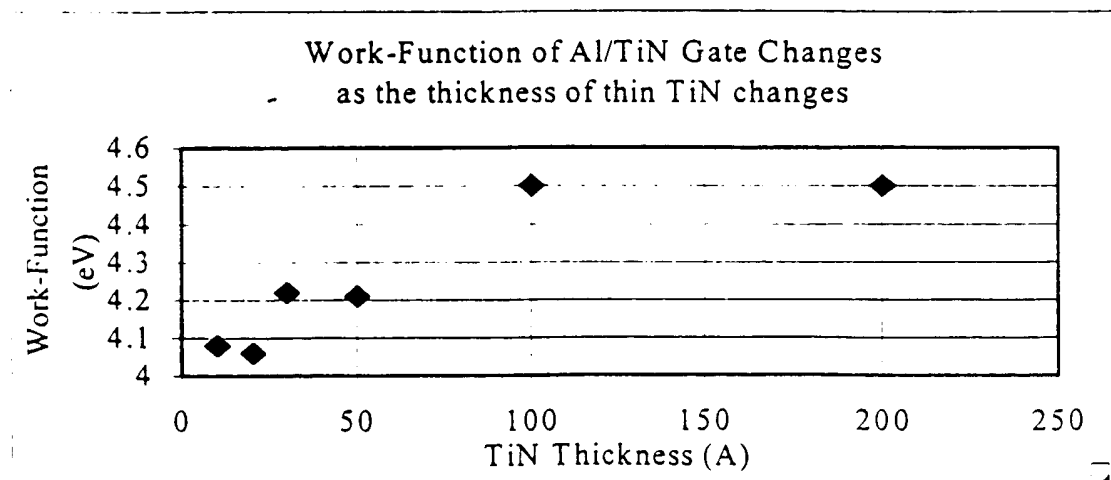


Fig. 4

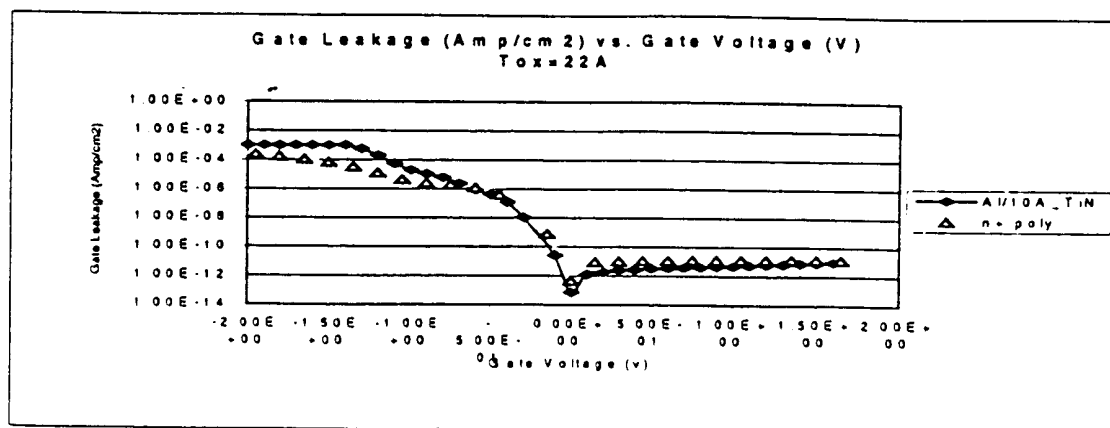
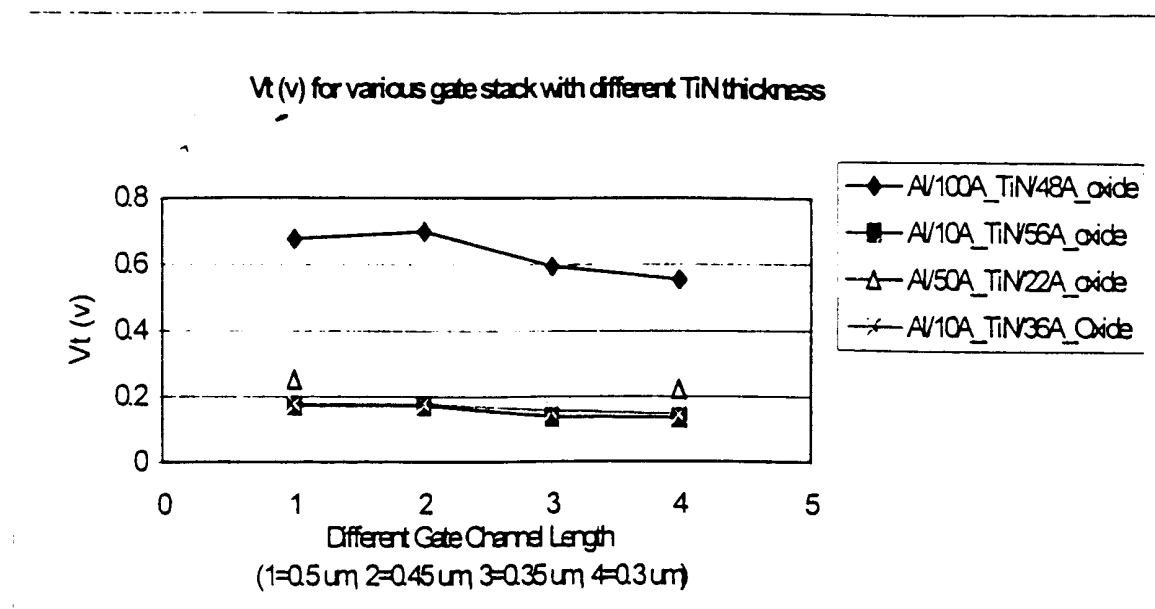


Fig.5

Quasi Static/High Frequency Capacitor Voltage
Curves for Al/20A_TiN/50A Oxide
Gate Stack

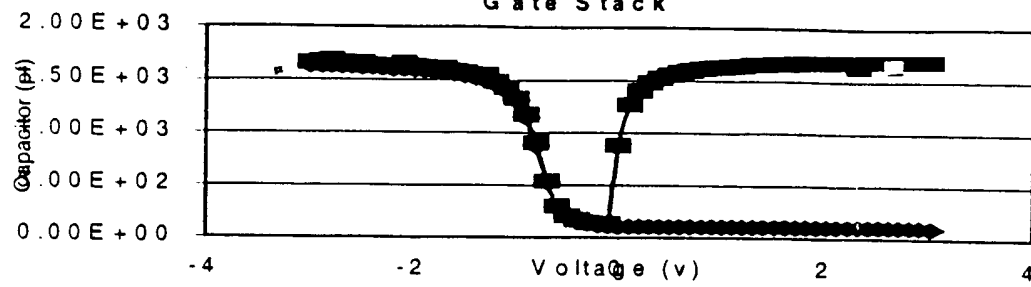


Fig.6

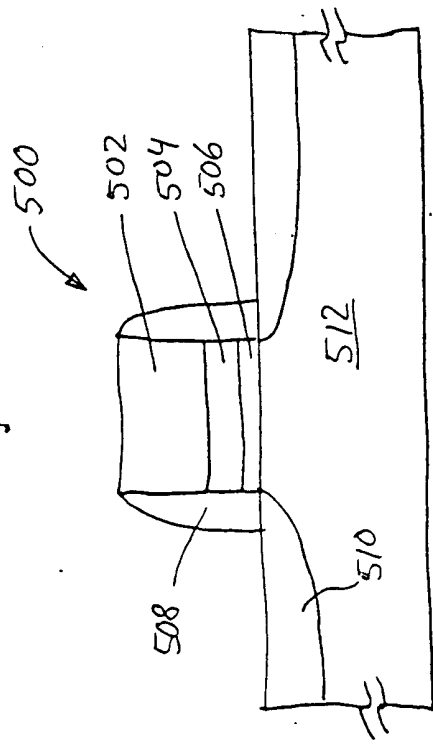


Fig. 7

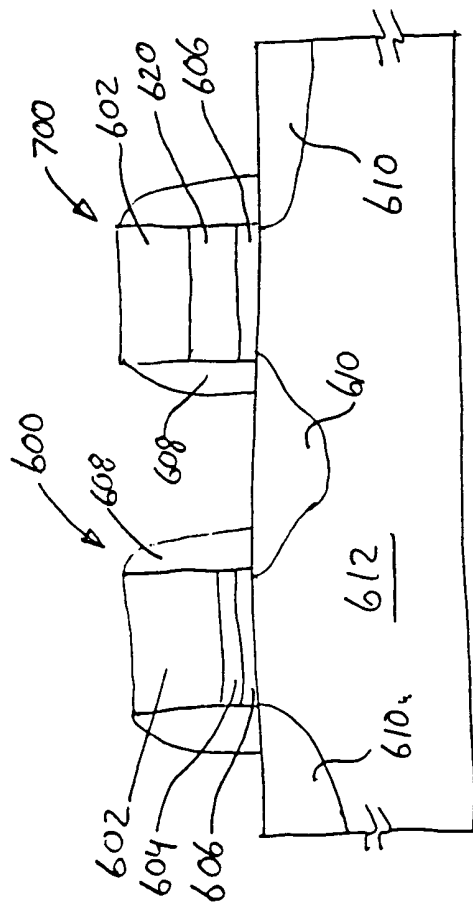


Fig. 8